Errata of K13126

Introduction to VLSI Systems: A Logic, Circuit, and System Perspective

Chapter 1.

- (Page 8, **Table 1-1**) The 0.35-μm process parameters are from MOSIS, both 0.25-μm and 0.18-μm process parameters are from TSMC, 0.13-μm process parameters are from IBM, and the rest process parameters are from PTM (http://ptm.asu.edu).
- (Page 9, line 4) "Second,..." $\longrightarrow$ "Second, to deliver a specific power, the currents passing through wires in DSM processes are greater than those in SM processes due to the reduction of the supply voltage in DSM processes."
- (Page 48, line 5 of Section 1.4.1) "Recall three important ...with DSM processes:..." $\longrightarrow$ "Recall that the three important issues in designing a VLSI system with DSM processes are..."

Chapter 2.

- (Page 73) Equation (2.31) $\longrightarrow$

$$C_j = AC_{j0}\left[1 - \frac{V}{\phi_0}\right]^{-m}$$

- (Page 73) Equation (2.32)) $\longrightarrow$

$$C_{j0} = \left(\frac{e\varepsilon_{si}}{2\phi_0}\frac{N_aN_d}{N_a+N_d}\right)^{1/2}$$

- (Page 75, the C_{j0} equation) "The C_{j0} equation $\longrightarrow$

$$\begin{aligned} C_{j0} &= \left(\frac{e\varepsilon_{si}}{2\phi_0}\frac{N_aN_d}{N_a+N_d}\right)^{1/2} \\ &= \left(\frac{1.6\times10^{-19}\times11.7\times8.854\times10^{-14}}{2\times0.86}\frac{5\times10^{18}\times10^{16}}{5\times10^{18}+10^{16}}\right)^{1/2} \\ &= 0.31\ \text{fF}/\mu\text{m}^2 \end{aligned}$$

- (Page 75, the C_j equation) "The C_j equation $\longrightarrow$

$$C_j = \frac{AC_{j0}}{[1-(V/\phi_0)]^m} = \frac{400\times0.31\ \text{fF}}{[1-(-2.5/0.86)]^{0.5}} = 60.7\ \text{fF}$$

- (Page 75, the C_{eq} equation) "The C_{eq} equation $\longrightarrow$

$$AC_{eq} = -\frac{AC_{j0}\phi_0}{(V_2-V_1)(1-m)}\left[\left(1-\frac{V_2}{\phi_0}\right)^{1-m} - \left(1-\frac{V_1}{\phi_0}\right)^{1-m}\right]$$

- (Page 83, line 8) "with zero gate voltage..." $\longrightarrow$ "with a gate voltage less than the desired value..."
- (Page 83, line 24) "2. The term ϕ_{GS} is the work function difference between..." $\longrightarrow$ "2. The term ϕ_{GS} is due to the work function difference between..."
- (Page 90, Equation(2.65)) "ϕ_0" $\longrightarrow$ "$2|\phi_{fp}|$"
- (Page 91, the last row of Table 2.3) "$1/k$" $\longrightarrow$ "k"
- (Page 100, the the first line) "the threshold slope of Figure 2.25(a) is" $\longrightarrow$ "the reciprocal of the slope of the above equation is defined as the *subthreshold slope* and is equal to"
- (Page 103, Equation (2.87)) $\mu_{eff} = \dfrac{A}{1+\left(\frac{E_{norm}}{B}\right)} \longrightarrow \mu_{eff} = \dfrac{A}{1+\left(\frac{E_{norm}}{B}\right)^n}$ where n is 1.6 for electrons and is 1.0 for holes.
- (Pages 103–104, Example 2-11) 1. $\mu_{eff} = 285$ cm^2/V-s $\longrightarrow \mu_{eff} = 259$ cm^2/V-s.
  2. $E_{norm} = 5.69\times10^5$ V/cm $\longrightarrow 8.94\times10^5$ V/cm. $\mu_{eff} = 88$ cm^2/V-s $\longrightarrow \mu_{eff} = 70$ cm^2/V-s.
- (Page 105, Equation (2.95)) the "-" in the denominator $\longrightarrow$ "+"
- (Page 125, **Problem 2-9**) "ϕ_G and ϕ_{Si} are the work function..." $\longrightarrow$ "$e\phi_G$ and $e\phi_{Si}$ are the work function..."

Chapter 3.

- (Page 138, the 4th line from bottom) "to pattern a dielectric layer at every..." $\longrightarrow$ "to pattern a phase-shift coating (i.e., a dielectric) layer at every..."

Chapter 5.

- (In this book) "Intrinsic delay" $\longrightarrow$ "Intrinsic time constant"
- (In this book) "Intrinsic propagation delay" $\longrightarrow$ "Intrinsic time constant"
- (Page 246, the 2nd line from the bottom) "$0.35\times^{-4}$" $\longrightarrow$ "0.35×10^{-4}"
- (Page 247, the 7th line) "$0.18\times^{-4}$" $\longrightarrow$ "0.18×10^{-4}"
- (Page 248, the 3rd, 6th, and 9th lines) "the zero-bias junction capacitance" $\longrightarrow$ "the junction capacitance"
- (Page 255, Equation (5.27)) "$I_{HL(avg)}$" $\longrightarrow$ "$I_{LH(avg)}$"
- (Page 257, the 1st line) "$I_{HL(avg)}$" $\longrightarrow$ "$I_{LH(avg)}$"
- (Page 265, the 7th line) "Mediate-length wire" $\longrightarrow$ "Moderate-length wire"
- (Page 285, **Figure 5.34**) Add fF to all capacitance values.

A new self-capacitance model: The following changes are derived from a new self-capacitance model by modifying the **Figure 5.17(b)** as depicted as follows.

- (Page 265, **Figure 5.17(b)**) the input "$2C_{OL}$" $\longrightarrow$ "$(1+\alpha)C_{OL}$" while the output "$2C_{OL}$" $\longrightarrow$ "$(1+\frac{1}{\alpha})C_{OL}$"

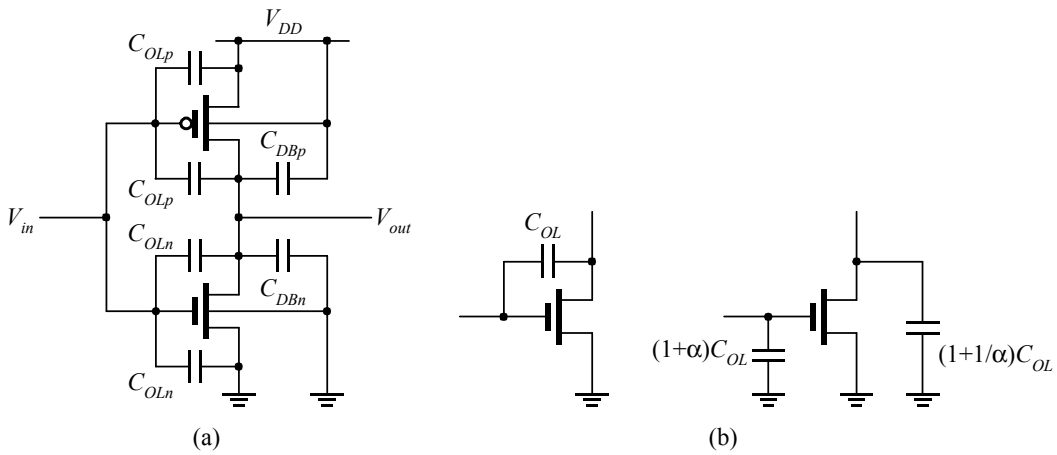


Figure 5.17: (a) The calculation of the self-loading capacitance in CMOS inverters. (b) Miller effect.

- (Page 264, Equation 5.42) $\longrightarrow$

$$\begin{aligned} C_{self-load} &= C_{DBn} + (1+1/\alpha)C_{OLn} + C_{DBp} + (1+1/\alpha)C_{OLp} \\ &= C_{jn}W_n + (1+1/\alpha)C_{ol}W_n + C_{jp}W_p + (1+1/\alpha)C_{ol}W_p \\ &= [C_j + (1+1/\alpha)C_{ol}](W_n + W_p) \\ &= C_{para}(W_n + W_p) \end{aligned}$$

where C_{jn} and C_{jp} are assumed to be the same and equal to C_j, and $C_{para} = C_j + (1+1/\alpha)C_{ol}$, where α is a positive number.

- (Page 265, **Table 5.5**) $\longrightarrow$

Process	0.35 μm	0.25 μm	0.18 μm	0.13 μm	90 nm	65 nm	45 nm	32 nm	Unit
τ_{inv}	25.3	21.71	14.78	13.03	9.06	5.74	4.74	3.23	ps
$C_{ox}L_{actual}$	1.43	1.26	1.18	1.21	0.83	1.02	0.74	0.56	fF/μm
C_g	2.91	2.78	3.45	1.85	2.1	1.72	1.57	1.21	fF/μm
C_{para}	4.65	4.31	3.72	1.89	2.68	4.27	4.45	4.14	fF/μm
γ_{inv}	1.6	1.55	1.08	1.02	1.28	2.48	2.84	3.42	
α	0.67	0.61	0.71	0.42	0.62	0.23	0.27	0.20	
C_{ol}	0.55	0.58	0.84	0.26	0.48	0.31	0.37	0.30	fF/μm
C_j	3.28	2.78	1.70	1.01	1.43	2.61	2.71	2.34	fF/μm

- (Page 266, Equation 5.44) $\longrightarrow$

$$\begin{aligned} C_G &= C_{Gn} + (2+\alpha)C_{OLn} + C_{Gp} + (2+\alpha)C_{OLp} \\ &= C_{ox}L_{actual}W_n + (2+\alpha)C_{ol}W_n + C_{ox}L_{actual}W_p + (2+\alpha)C_{ol}W_p \\ &= [C_{ox}L_{actual} + (2+\alpha)C_{ol}](W_n + W_p) \\ &= C_g(W_n + W_p) \end{aligned}$$

where $C_g = C_{ox}L_{actual} + (2+\alpha)C_{ol}$.

- (Page 267, Equation 5.47) $\longrightarrow$

$$
\begin{aligned}
t_{pd} &= \tau_{inv}\left(\frac{C_j + (1+1/\alpha)C_{ol}}{C_g} + \frac{C_{out}}{C_{in}}\right) \\
&= \tau_{inv}\left(\frac{C_j + (1+1/\alpha)C_{ol}}{C_g}\right) + \tau_{inv}\cdot h \\
&= a + b\cdot h
\end{aligned} \tag{1}
$$

where $h = C_{out}/C_{in}$ is called the *fan-out* of the inverter, $C_{in} = C_g(W_n + W_p)$, $C_{self-load} = [C_j + (1+1/\alpha)C_{ol}](W_n + W_p)$, and b is the intrinsic time constant τ_{inv},

- (Page 269, **Table 5.6**) $\longrightarrow$

Process	0.35 μm	0.25 μm	0.18 μm	0.13 μm	90 nm	65 nm	45 nm	32 nm	Unit
Without junction capacitance									
$t_{pd}(f=8)$	215	186	127	111	78	51.5	43	30.3	ps
$t_{pd}(f=1)$	37.4	33.8	23.4	19.4	14.5	11.4	9.98	7.91	ps
a_{nocj}	12.03	12.06	8.6	6.31	5.43	5.67	5.26	4.71	ps
b	25.37	21.74	14.8	13.09	9.07	5.73	4.72	3.20	ps
With junction capacitance									
$t_{pd}(f=8)$	242	207	134	117	83.9	60.2	51.5	37.1	ps
$t_{pd}(f=1)$	65.4	55.3	30.7	26.3	20.6	20.0	18.2	14.3	ps
a_{cj}	40.4	33.63	15.94	13.34	11.56	14.26	13.44	11.04	ps
b	25.23	21.67	14.76	12.96	9.04	5.74	4.76	3.26	ps

- (Page 269, Solution of **Example 5-11**) $\longrightarrow$

Solution: From Equation (5.45) and the equivalent on-resistance from Table 5.1, we obtain the value of C_g as

$$C_g = \frac{\tau_{inv}}{3R_{eqn}L_n} = \frac{14.78}{3\times 7.93\times 0.18} = 3.45 \text{ fF}/\mu\text{m}$$

To calculate α, we need to solve the following two equations simultaneously:

$$
\begin{aligned}
3.45 &= 1.18 + (2+\alpha)C_{ol} \\
8.6 &= 14.78 \times \left(\frac{(1+1/\alpha)C_{ol}}{3.45}\right)
\end{aligned}
$$

The resulting α is 0.71 and the overlap capacitance C_{ol} is 0.84 fF/μm.

The parasitic capacitance C_{para} can be calculated as follows:

$$C_{para} = C_g \times \frac{a_{cj}}{\tau_{inv}} = 3.45 \times \frac{15.94}{14.78} = 3.72 \ \text{ fF}/\mu\text{m}$$

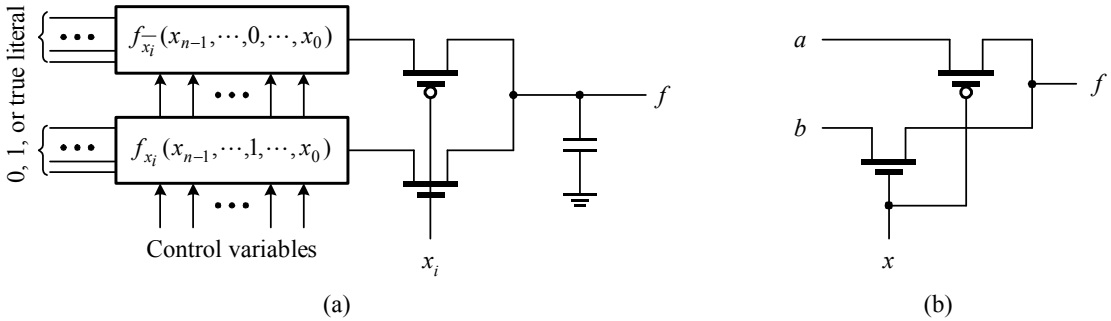
The junction capacitance C_j can be found from the parasitic capacitance C_{para} and is found to be

$$C_j = 3.72 - \left(1 + \frac{1}{0.71}\right) \times 0.84 = 1.70 \ \text{ fF}/\mu\text{m}$$

Hence, the capacitances C_{ol}, C_{para}, and C_j are 0.84, 3.72, and 1.70 fF/μm, respectively.

Chapter 7.

- (Page 345, **Figure 7.13**) $\longrightarrow$



- (Page 345, the 3rd line) "a $f/\bar{f}$ network" $\longrightarrow$ "a freeform- or uniform-tree network"

- (Page 345, from the 7th line to the line before **Example 7-9**) "Generally, a GDI logic circuit" $\longrightarrow$ "As depicted in Figure 7.13(b), a single-stage GDI logic circuit generally"

- (Page 345, Equation (7.33)) $\longrightarrow$

$$f(x,y) = f(0,y)\cdot\bar{x} + f(1,y)\cdot x = a\cdot\bar{x} + b\cdot x$$

- (Page 345, the two lines after Equation (7.33)) $\longrightarrow$ "where $\bar{x}$ is implemented by a pMOS switch while x is implemented by an nMOS switch. a and b are the residues of $f(x,y)$ with respect to literals $\bar{x}$ and x, respectively. An illustration of GDI logic is explored in the following example."

- (Page 345, the 5th line from the bottom) "the uniform-tree network" $\longrightarrow$ "the freeform- and uniform-tree networks"

Chapter 8.

- (Page 378, the 2nd line from the bottom of the last paragraph) "expressed as follows:" $\longrightarrow$ "expressed as follows as the TG switch is off:"

- (Page 378, the 2nd line from the bottom of the last paragraph) "Equation (8.1)" $\longrightarrow$

$$C_{TG(in)} = C_{TG(out)} = (C_j + C_{ol})(W_n + W_p) = 2(C_j + C_{ol})W$$

- (page 379, the last line) "delay at the output." $\longrightarrow$ "delay at the output of the TG switch."

- (page 380, **Figure 8.6**) In **Figure 8.6(a)**, add "x" at the input node of the output inverter; In **Figure 8.6(b)**, "V_{out}" $\longrightarrow$ "V_x."

- (page 380, Equation (8.3)) $\longrightarrow$

$$C_{TG(in)} = C_{TG(out)} = (C_j + C_{ol})(W_n + W_p) = 2(C_j + C_{ol})W$$

- (page 380, Equation (8.4)) $\longrightarrow$

$$C_{TG(in)} = C_{TG(out)} = (C_j + C_{ol})(W_n + W_p) + \frac{1}{2}C_{ox}L_{actual}(W_n + W_p)$$
$$= 2(C_j + C_{ol})W + C_{ox}L_{actual}W$$

- (page 380, the second line of Equation (8.5)) $\longrightarrow$

$$= R_{inv}\left[3C_{para}W + 2(C_j + C_{ol})W + C_{ox}L_{actual}W\right] +$$
$$(R_{inv} + R_{TG})\left[2(C_j + C_{ol})W + C_{ox}L_{actual}W + 3C_gW\right]$$

- (Page 395, the 4th and 5th lines in paragraph two) "to be equal before the nMOS switch is on." $\longrightarrow$ "to be equal since in this case the nMOS switch cannot be actually turned on."
- (Page 395, the 2nd line from the bottom of paragraph two) "$[Q_{total} - C_1(V_G - V_{Tn})]/C_2$" $\longrightarrow$ "$[Q_{total} - C_1(V_G - V_{Tn} - V_1)]/C_2$ "
- (Page 396, the 1st line) "which is above $V_G - V_{Tn} = 1.8 - 0.7 = 1.1$ V." $\longrightarrow$ "which is above $V_G - V_{Tn} = 1.8 - 0.7 = 1.1$ V if V_{Tn} is assumed to be 0.7 V."

Chapter 9.

- (Page 466, **Figure 9.42**) the *clk* and $\overline{clk}$ associated with the two middle TG switches are interchanged.
- (Page 466, the 8th line) "input data as the clock *clk* is low." $\longrightarrow$ "input data as the clock *clk* is high."
- (Page 473, the 3rd line) "there are many time constraints that" $\longrightarrow$ "there are many timing constraints that"
- (In this chapter and the rest of the book) "t_q" $\longrightarrow$ "t_{cq}"
- (In this chapter and the rest of the book) "$t_{q(min)}$" $\longrightarrow$ "$t_{cq(min)}$"
- (Page 478, Equation (9.18)) "$+t_{skew}$" $\longrightarrow$ "$-t_{skew}$"
- (Page 479, Equation (9.19)) "$+t_{skew,i}$" $\longrightarrow$ "$-t_{skew,i}$"

Chapter 11.

- (Page 587, the 9th line) "...$\times 0.18 = 5.52$ fF" $\longrightarrow$ "...$\times 0.18/2 = 2.76$ fF"
- (Page 587, the 13th line) "5.52" $\longrightarrow$ "2.76"
- (Page 609, **Figure 11.40**) $\longrightarrow$

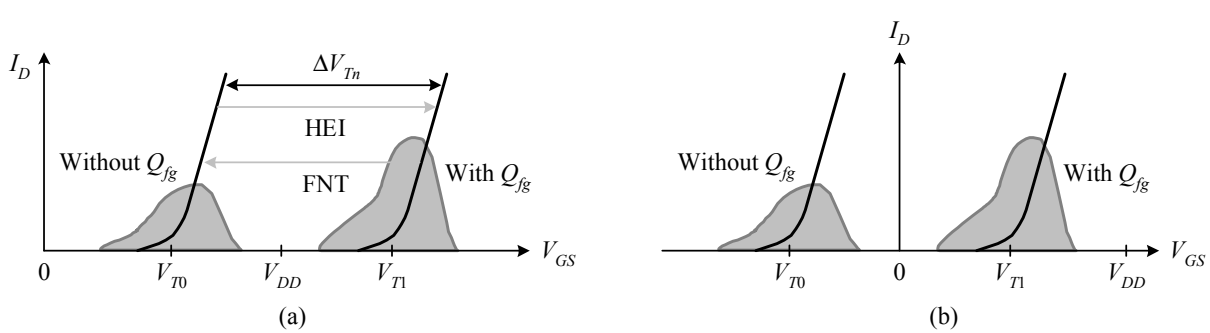


Figure 11.40: The threshold voltage change of the ETOX transistor before and after programming for (a) NOR Flash memory and (b) NAND Flash memory.

- (Page 611, the 4th line from the bottom) "a value much less than V_{DD}" $\longrightarrow$ "a value much higher than V_{DD}"

Chapter 12.

- (Page 650, the 4th paragraph) $\longrightarrow$

  At present, a computer (usually a microprocessor or a microcomputer) or computers are often embedded into an electronic system. In such a system, the computer or computers are primarily used as components like the others to simplify the system design and to provide flexibility; the user of the system is not even aware of the presence of the computer or computers inside the system. A computer used in this way is referred to as an *embedded system*. In other words, an embedded system is a computer system used as a component for designing a system.

- (Page 651, the last paragraph) $\longrightarrow$

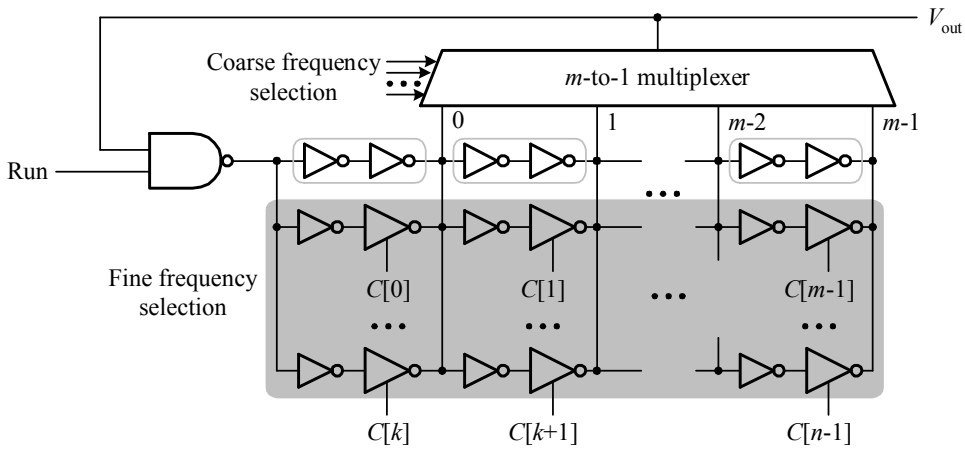
  Because all of the three platform-based systems introduced above use computer(s) as components to build systems, and these systems are founded on silicon, they are system-on-a-chip (SoC). In other words, an SoC is a system containing one or more embedded systems on silicon. The design issues of platform-based systems involve the system-level hardware and software co-design, which is beyond the scope of this book and hence we omit it here.

Chapter 13.

- (Page 688, Equation 13.28) "$R_{eqn}C_GM$" $\longrightarrow$ "$R_{int}C_GM$"
- (Page 689, Equation 13.31) "$R_{int}C_{int}l$" $\longrightarrow$ "$R_{eqn}C_{int}l$"
- (Page 696, The line before Equation 13.46) "The propagation time per unit length ...." $\longrightarrow$ "The propagation time (t_p) of a transmission line with length l is equal to the square root of the product of L and C:"
- (Page 696, Equation 13.46) "$t_p = \sqrt{L_{int}C_{int}}$" $\longrightarrow$ "$t_p = \sqrt{LC} = l\sqrt{L_{int}C_{int}}$"
- (Page 708, the 12th line) "$(R_i + R_{w_i} \cdot C_{i+1}$" $\longrightarrow$ "$(R_i + R_{w_i}) \cdot C_{i+1}$"

Chapter 14.

- (Page 739, **Figure 14.30**) $\longrightarrow$



Chapter 16.

- (Page 781, the 16th line) "from 75° to 85°." ⟶ "from 75°C to 85°C."

Appendix.

- (Page 814, the 3rd line in Section **A.1.3.1**) "In industry, ... by logic synthesis tools." ⟶ "In industry, the term *register-transfer level* (RTL) *code* is often used to mean that an RTL module (i.e., constructed with the RTL components) is modeled in behavioral, dataflow, structural, or mixed style on condition that the resulting description must be acceptable by logic synthesis tools."